Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph numbers [0024], [0027], [0077] and [0090], with the following rewritten paragraphs:

[0024] FIGURE 7 is a diagrammatic representation of an Accumulated Maximal Ratio Combining (A-MRC) algorithm processing unit[[s]] in accordance with an exemplary embodiment;

[0027] FIGURE 10 is a diagrammatic representation of the Accumulated Maximal Ratio Combining (A-MRC) algorithm processing unit[[s]] of FIGURE 7 in greater detail;

[0077] In an exemplary embodiment, a PN sequence 104 is received by shift register[[s]] 106. Shift register[[s]] 106 direct**ly** processe[[d]]**s** chips from the PN sequence 104 to a number of RAM devices (e.g., RAM 1-32). RAM device 108 includes, for example, partial sums of chips 1-4. RAM device 110 includes partial sums of chips 5-8. RAM device 112 includes partial sums of chips 125-128. Correlations from the RAM devices are combined using a combining apparatus 124.

[0090] FIGURE 20 illustrates an exemplary implementation of the convergent searcher operation by the processor 20. The convergent searcher 90 receives samples including a phase rotation from a subtraction of samples from the sample buffers 22 and known paths from a FIR block 98. FIR (finite impulse response) block 98 is a pulse shaping filter. Known ~~paths~~ **pilots** 94 are re-modulated by a re-modulator 96 and provided to the FIR block 98 along with channel estimates.